

	L #	Hits	Search Text	DBs
1	L1	1160	(cache near5 coheren\$3) and (shared adj1 memory) and (((multi multiple) adj1 processor) multiprocessor)	USPAT; US-PGPUB
2	L2	48	((cache near5 coheren\$3) and (shared adj1 memory) and (((multi multiple) adj1 processor) multiprocessor)).ab,ti.	USPAT; US-PGPUB
3	L4	4	2 and 3	USPAT; US-PGPUB
4	L3	62	cache near10 line near10 lock\$3 and 1	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20040 05987 7 A1	<input type="checkbox"/>	Method and apparatus for implementing cache state as history of read/write shared data	711/144
2	US 20040 05485 5 A1	<input checked="" type="checkbox"/>	Shared memory multiprocessor performing cache coherence control and node controller therefor	711/147
3	US 20040 03474 7 A1	<input checked="" type="checkbox"/>	Scalable cache coherent distributed shared memory processing system	711/148
4	US 20030 16354 3 A1	<input checked="" type="checkbox"/>	Method and system for cache coherence in DSM multiprocessor system without growth of the sharing vector	709/214
5	US 20030 11540 2 A1	<input checked="" type="checkbox"/>	Multiprocessor system	711/1
6	US 20020 16603 2 A1	<input checked="" type="checkbox"/>	Method for verifying abstract memory models of shared memory multiprocessors	711/141
7	US 20020 14406 3 A1	<input checked="" type="checkbox"/>	Multiprocessor cache coherence management	711/141
8	US 20020 13869 8 A1	<input checked="" type="checkbox"/>	System and method for caching directory information in a shared memory multiprocessor system	711/130
9	US 20020 13367 4 A1	<input checked="" type="checkbox"/>	Bandwidth-adaptive, hybrid, cache-coherence protocol	711/141
10	US 20020 12920 8 A1	<input checked="" type="checkbox"/>	System for handling coherence protocol races in a scalable shared memory system based on chip multiprocessing	711/141
11	US 20020 10002 0 A1	<input checked="" type="checkbox"/>	Method for maintaining cache coherency in software in a shared memory system	717/124
12	US 20020 10001 9 A1	<input checked="" type="checkbox"/>	Software shared memory bus	717/124
13	US 20020 07307 1 A1	<input checked="" type="checkbox"/>	Transactional memory for distributed shared memory multi-processor computer systems	707/1
14	US 20020 05300 4 A1	<input checked="" type="checkbox"/>	ASYNCHRONOUS CACHE COHERENCE ARCHITECTURE IN A SHARED MEMORY MULTIPROCESSOR WITH POINT-TO-POINT LINKS	711/119
15	US 20020 05291 4 A1	<input checked="" type="checkbox"/>	SOFTWARE PARTITIONED MULTI-PROCESSOR SYSTEM WITH FLEXIBLE RESOURCE SHARING LEVELS	709/203
16	US 20010 05205 4 A1	<input checked="" type="checkbox"/>	APPARATUS AND METHOD FOR PARTITIONED MEMORY PROTECTION IN CACHE COHERENT SYMMETRIC MULTIPROCESSOR SYSTEMS	711/147
17	US 20010 00587 3 A1	<input checked="" type="checkbox"/>	Shared memory multiprocessor performing cache coherence control and node controller therefor	710/305

	Document ID	U	Title	Current OR
18	US 67116 62 B2	<input checked="" type="checkbox"/>	Multiprocessor cache coherence management	711/204
19	US 66752 62 B1	<input checked="" type="checkbox"/>	Multi-processor computer system with cache-flushing system using memory recall	711/135
20	US 66369 49 B2	<input checked="" type="checkbox"/>	System for handling coherence protocol races in a scalable shared memory system based on chip multiprocessing	711/141
21	US 66369 26 B2	<input checked="" type="checkbox"/>	Shared memory multiprocessor performing cache coherence control and node controller therefor	710/305
22	US 66339 45 B1	<input checked="" type="checkbox"/>	Fully connected cache coherent multiprocessing systems	710/316
23	US 65464 71 B1	<input checked="" type="checkbox"/>	Shared memory multiprocessor performing cache coherency	711/148
24	US 65429 26 B2	<input checked="" type="checkbox"/>	Software partitioned multi-processor system with flexible resource sharing levels	709/213
25	US 65264 81 B1	<input checked="" type="checkbox"/>	Adaptive cache coherence protocols	711/147
26	US 65164 42 B1	<input checked="" type="checkbox"/>	Channel interface and protocols for cache coherency in a scalable symmetric multiprocessor system	714/776
27	US 65104 96 B1	<input checked="" type="checkbox"/>	Shared memory multiprocessor system and method with address translation between partitions and resetting of nodes included in other partitions	711/147
28	US 64571 00 B1	<input checked="" type="checkbox"/>	Scalable shared-memory multi-processor computer system having repetitive chip structure with efficient busing and coherence controls	711/119
29	US 64496 99 B2	<input checked="" type="checkbox"/>	Apparatus and method for partitioned memory protection in cache coherent symmetric multiprocessor systems	711/147
30	US 63602 31 B1	<input checked="" type="checkbox"/>	Transactional memory for distributed shared memory multi-processor computer systems	707/201
31	US 63569 83 B1	<input checked="" type="checkbox"/>	System and method providing cache coherency and atomic memory operations in a multiprocessor computer architecture	711/145
32	US 63413 37 B1	<input checked="" type="checkbox"/>	Apparatus and method for implementing a snoop bus protocol without snoop-in and snoop-out logic	711/146
33	US 62090 64 B1	<input checked="" type="checkbox"/>	Cache coherence unit with integrated message passing and memory protection for a distributed, shared memory multiprocessor system	711/141
34	US 61483 75 A	<input checked="" type="checkbox"/>	Hierarchical bus simple COMA architecture for shared memory multiprocessors having a bus directly interconnecting caches between nodes	711/130
35	US 60887 70 A	<input checked="" type="checkbox"/>	Shared memory multiprocessor performing cache coherency	711/148
36	US 60887 68 A	<input checked="" type="checkbox"/>	Method and system for maintaining cache coherence in a multiprocessor-multicache environment having unordered communication	711/141
37	US 58954 86 A	<input checked="" type="checkbox"/>	Method and system for selectively invalidating cache lines during multiple word store operations for memory coherence	711/121
38	US 58359 50 A	<input checked="" type="checkbox"/>	Self-validation method for reducing coherence overheads in a bus-based shared-memory multiprocessor apparatus	711/144
39	US 58227 63 A	<input checked="" type="checkbox"/>	Cache coherence protocol for reducing the effects of false sharing in non-bus-based shared-memory multiprocessors	711/141
40	US 58095 36 A	<input checked="" type="checkbox"/>	Method for reducing the number of coherency cycles within a directory-based cache coherency memory system utilizing a memory state cache	711/144

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41	US 58025 82 A	<input checked="" type="checkbox"/>	Explicit coherence using split-phase controls	711/152
42	US 57522 58 A	<input checked="" type="checkbox"/>	Encoding method for directory state in cache coherent distributed shared memory system	711/120
43	US 57377 57 A	<input checked="" type="checkbox"/>	Cache tag system for use with multiple processors including the most recently requested processor identification	711/145
44	US 57154 28 A	<input checked="" type="checkbox"/>	Apparatus for maintaining multilevel cache hierarchy coherency in a multiprocessor computer system	711/141
45	US 55112 26 A	<input checked="" type="checkbox"/>	System for generating snoop addresses and conditionally generating source addresses whenever there is no snoop hit, the source addresses lagging behind the corresponding snoop addresses	711/146
46	US 54044 83 A	<input checked="" type="checkbox"/>	Processor and method for delaying the processing of cache coherency transactions during outstanding cache fills	711/144
47	US 52768 28 A	<input checked="" type="checkbox"/>	Methods of maintaining cache coherence and processor synchronization in a multiprocessor system using send and receive instructions	709/248
48	US 52747 87 A	<input type="checkbox"/>	Method of copy-back cache coherence control and tightly coupled multi-processor system with split transfer system bus	711/143

	Document ID	U	Title	Current OR
1	US 20040 05989 3 A1	<input type="checkbox"/>	System and method to automatically stack and unstack java local variables	712/208
2	US 20030 22597 9 A1	<input checked="" type="checkbox"/>	Methods and apparatus for speculative probing of a remote cluster	711/141
3	US 20030 22597 8 A1	<input checked="" type="checkbox"/>	Methods and apparatus for speculative probing of a remote cluster	711/141
4	US 20030 21274 1 A1	<input checked="" type="checkbox"/>	Methods and apparatus for responding to a request cluster	709/203
5	US 20030 21065 5 A1	<input checked="" type="checkbox"/>	Methods and apparatus for responding to a request cluster	370/244
6	US 20030 18251 4 A1	<input checked="" type="checkbox"/>	Methods and apparatus for speculative probing with early completion and delayed request	711/141
7	US 20030 18250 9 A1	<input checked="" type="checkbox"/>	Methods and apparatus for speculative probing at a request cluster	711/119
8	US 20030 18250 8 A1	<input checked="" type="checkbox"/>	Methods and apparatus for speculative probing with early completion and early request	711/118
9	US 20030 16364 2 A1	<input checked="" type="checkbox"/>	Shared cache line update mechanism	711/121
10	US 20030 06589 4 A1	<input checked="" type="checkbox"/>	Technique for implementing a distributed lock in a processor-based device	711/152
11	US 20030 04649 5 A1	<input checked="" type="checkbox"/>	Streamlined cache coherency protocol system and method for a multiple processor single chip device	711/141
12	US 20030 02379 4 A1	<input checked="" type="checkbox"/>	Cache coherent split transaction memory bus architecture and protocol for a multi processor chip device	710/105
13	US 20020 17430 5 A1	<input checked="" type="checkbox"/>	Method and apparatus for controlling memory storage locks based on cache line ownership	711/145
14	US 20020 14787 2 A1	<input checked="" type="checkbox"/>	Sequentially performed compound compare-and-swap	710/200
15	US 20010 05205 3 A1	<input checked="" type="checkbox"/>	Stream processing unit for a multi-streaming processor	711/138
16	US 66944 11 B2	<input checked="" type="checkbox"/>	Technique for implementing a distributed lock in a processor-based device	711/152
17	US 66752 62 B1	<input checked="" type="checkbox"/>	Multi-processor computer system with cache-flushing system using memory recall	711/135
18	US 66256 98 B2	<input checked="" type="checkbox"/>	Method and apparatus for controlling memory storage locks based on cache line ownership	711/141

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19	US 64938 09 B1	<input checked="" type="checkbox"/>	Maintaining order of write operations in a multiprocessor for memory consistency	711/167
20	US 64809 18 B1	<input checked="" type="checkbox"/>	Linger locks with fairness control for multi-node computer systems	710/200
21	US 64738 19 B1	<input checked="" type="checkbox"/>	Scalable interruptible queue locks for shared-memory multiprocessor	710/200
22	US 64601 24 B1	<input checked="" type="checkbox"/>	Method of using delays to speed processing of inferred critical program portions	711/163
23	US 64601 22 B1	<input checked="" type="checkbox"/>	System, apparatus and method for multi-level cache in a multi-processor/multi-controller environment	711/154
24	US 64571 00 B1	<input checked="" type="checkbox"/>	Scaleable shared-memory multi-processor computer system having repetitive chip structure with efficient busing and coherence controls	711/119
25	US 64570 87 B1	<input checked="" type="checkbox"/>	Apparatus and method for a cache coherent shared memory multiprocessing system	710/305
26	US 63895 15 B1	<input checked="" type="checkbox"/>	System and method for avoiding deadlocks utilizing split lock operations to provide exclusive access to memory during non-atomic operations	711/141
27	US 63743 29 B1	<input checked="" type="checkbox"/>	High-availability super server	711/141
28	US 63569 83 B1	<input checked="" type="checkbox"/>	System and method providing cache coherency and atomic memory operations in a multiprocessor computer architecture	711/145
29	US 62267 14 B1	<input checked="" type="checkbox"/>	Method for invalidating cache lines on a sharing list	711/119
30	US 61417 34 A	<input checked="" type="checkbox"/>	Method and apparatus for optimizing the performance of LDxL and STxC interlock instructions in the context of a write invalidate protocol	711/144
31	US 60947 09 A	<input checked="" type="checkbox"/>	Cache coherence for lazy entry consistency in lockup-free caches	711/141
32	US 60921 56 A	<input checked="" type="checkbox"/>	System and method for avoiding deadlocks utilizing split lock operations to provide exclusive access to memory during non-atomic operations	711/145
33	US 60650 77 A	<input checked="" type="checkbox"/>	Apparatus and method for a cache coherent shared memory multiprocessing system	710/100
34	US 60413 76 A	<input checked="" type="checkbox"/>	Distributed shared memory system having a first node that prevents other nodes from accessing requested data until a processor on the first node controls the requested data	710/108
35	US 60264 61 A	<input checked="" type="checkbox"/>	Bus arbitration system for multiprocessor architecture	710/244
36	US 60062 99 A	<input checked="" type="checkbox"/>	Apparatus and method for caching lock conditions in a multi-processor system	710/108
37	US 60000 07 A	<input checked="" type="checkbox"/>	Caching in a multi-processor computer system	711/105
38	US 59875 49 A	<input checked="" type="checkbox"/>	Method and apparatus providing short latency round-robin arbitration for access to a shared resource	710/107
39	US 59833 26 A	<input checked="" type="checkbox"/>	Multiprocessing system including an enhanced blocking mechanism for read-to-share-transactions in a NUMA mode	711/147
40	US 59788 74 A	<input checked="" type="checkbox"/>	Implementing snooping on a split-transaction computer system bus	710/107
41	US 59601 79 A	<input checked="" type="checkbox"/>	Method and apparatus extending coherence domain beyond a computer system bus	710/107

	Document ID	U	Title	Current OR
42	US 59110 52 A	<input checked="" type="checkbox"/>	Split transaction snooping bus protocol	710/113
43	US 59000 20 A	<input checked="" type="checkbox"/>	Method and apparatus for maintaining an order of write operations by processors in a multiprocessor computer to maintain memory consistency	711/167
44	US 58931 51 A	<input checked="" type="checkbox"/>	Method and apparatus for maintaining cache coherency in a computer system with a highly pipelined bus and multiple conflicting snoop requests	711/140
45	US 58902 00 A	<input checked="" type="checkbox"/>	Method and apparatus for maintaining cache coherency in a computer system with a highly pipelined bus and multiple conflicting snoop requests	711/108
46	US 58871 46 A	<input checked="" type="checkbox"/>	Symmetric multiprocessing computer with non-uniform memory access architecture	710/104
47	US 58754 64 A	<input checked="" type="checkbox"/>	Computer system with private and shared partitions in cache	711/129
48	US 58646 57 A	<input checked="" type="checkbox"/>	Main memory system and checkpointing protocol for fault-tolerant computer system	714/15
49	US 58601 59 A	<input checked="" type="checkbox"/>	Multiprocessing system including an apparatus for optimizing spin--lock operations	711/151
50	US 58290 33 A	<input checked="" type="checkbox"/>	Optimizing responses in a coherent distributed electronic system including a computer system	711/141
51	US 58227 63 A	<input checked="" type="checkbox"/>	Cache coherence protocol for reducing the effects of false sharing in non-bus-based shared-memory multiprocessors	711/141
52	US 58025 78 A	<input checked="" type="checkbox"/>	Multinode computer system with cache for combined tags	711/147
53	US 57969 39 A	<input checked="" type="checkbox"/>	High frequency sampling of processor performance counters	714/47
54	US 57872 67 A	<input checked="" type="checkbox"/>	Caching method and circuit for a memory system with circuit module architecture	711/105
55	US 57784 22 A	<input checked="" type="checkbox"/>	Data processing system memory controller that selectively caches data associated with write requests	711/117
56	US 57519 39 A	<input checked="" type="checkbox"/>	Main memory system and checkpointing protocol for fault-tolerant computer system using an exclusive-or memory	714/15
57	US 57456 72 A	<input checked="" type="checkbox"/>	Main memory system and checkpointing protocol for a fault-tolerant computer system using a read buffer	714/6
58	US 57375 14 A	<input checked="" type="checkbox"/>	Remote checkpoint memory system and protocol for fault-tolerant computer system	714/13
59	US 56780 26 A	<input checked="" type="checkbox"/>	Multi-processor data processing system with control for granting multiple storage locks in parallel and parallel lock priority and second level cache priority queues	711/152
60	US 55749 22 A	<input checked="" type="checkbox"/>	Processor with sequences of processor instructions for locked memory updates	712/220
61	US 52300 70 A	<input checked="" type="checkbox"/>	Access authorization table for multi-processor caches	711/145
62	US 47759 55 A	<input checked="" type="checkbox"/>	Cache coherence mechanism based on locking	711/145